September 18, 2026

Active Track:

Wideband Small-Signal Amplifier Design Competition
～ Toward the Standardization of Next-Generation Ultra-Wideband Communications ～

■ Requirement for applicants: student
■ Preliminary review: Required
#Details of the preliminary screening will be sent via email after registration.

1. Specification requirement

- Performance
  (a) The amplifier shall provide a gain of 10 dB or higher at 5 GHz.
- Board Size
  (a) The amplifier shall be implemented on a board of less than 60 mm × 30 mm × 30 mm.
  (b) Protruding parts such as connectors are excluded from the size specification (see Fig. 2).

2. Evaluation rules

Scores are assigned according to ranking in the following three evaluation categories.

- (a) Fractional bandwidth (FBW)
- (b) Gain
- (c) Board Size

The score for (a) FBW and (b) Gain is 20 points, and the score for (c) Board Size is 10 points. These correspond to the base scores, M where M=20 for (a) FBW and (b) Gain, and M=10 for (c) Board Size.

The score is determined by the rank of each item. In case of a tie, priority is given in the following order: (a) Bandwidth → (b) Gain → (c) Size. If the number of teams meeting the required specifications is N, the score for the k-th place in each category is given by

- $(N + 1 - k) \times \frac{M}{N}$ points.

The participant with the highest total score is declared the winner. Any submission that fails to meet even one of the required specifications will receive zero points for all evaluation items.

(a) Fractional Bandwidth (FBW)

The target bandwidth is defined as the bandwidth of the continuous frequency range including 5 GHz over which the gain is within 3 dB of the maximum gain and is greater than or equal to 10 dB. (see Fig. 1)
The fractional bandwidth is calculated as:

$$\text{Fractional Bandwidth (FBW)} = \frac{F_H - F_L}{(F_H + F_L)/2}$$

Where:

- F_H: Upper frequency limit of the target bandwidth
- F_L: Lower frequency limit of the target bandwidth

Constraints:

- $F_L \geq 100\text{MHz}$
- $F_H \leq 18{,}000\text{MHz}$
- A wider value results in a higher score.

(b) Gain

The gain is evaluated based on the maximum gain within the specified bandwidth.

- A higher value results in a higher score.

(c) Size

The size is evaluated based on the board area:

$$X\ (\leq 60\ \text{mm}) \times Y\ (\leq 30\ \text{mm})\ [\text{mm}^2]$$

- A smaller area results in a higher score.

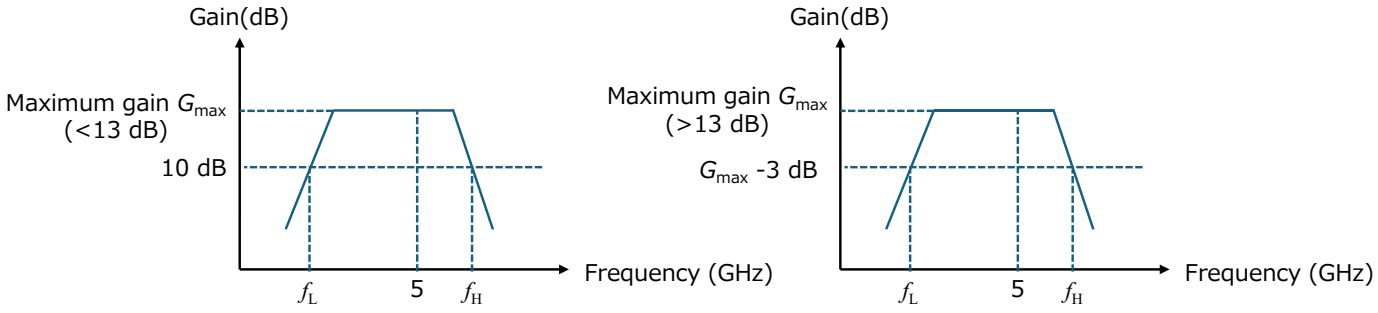

Figure 1. Evaluation of gain and bandwidth

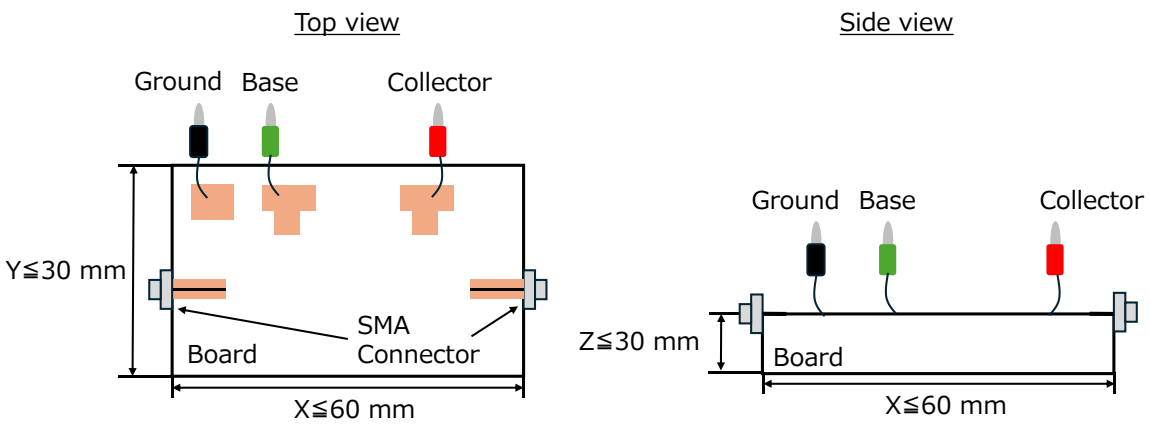

Figure 2. Evaluation of board size (top and side view)

3. Design conditions

(a) Transistor

The following transistor must be used: BFP740F

(DigiKey)

BFP740FH6327XTSA1 Infineon Technologies | Bipolar RF Transistors | DigiKey

(Mouser)

BFP740FH6327XTSA1 Infineon Technologies | Mouser

(b) Configuration

Single-stage amplifier only.

(c) Bias Circuit

A bias circuit must be included.

Use a ϕ 4 mm banana plug (male) for bias connections.

(d) DC Blocking

Input and output ports must include DC blocking capacitors or couplers.

(e) Collector Bias Conditions

- Collector voltage: ≤ 3 V
- Collector current: ≤ 15 mA

(f) Input Power

Maximum input power for CW measurement: less than -20 dBm

(g) I/O Connectors

- 50Ω SMA female connectors (Standard SMA, 1/4-36 UNS thread) must be used

(h) Reflection Gain

With bias applied:

- Input/output reflection gain must be less than 0 dB
- Frequency range: 100 MHz–18 GHz

(i) Stability Factor

- Stability factor $K > 1$
- Frequency range: 100 MHz–18 GHz

(j) Board Shape

Must be rectangular or square.

(k) Grounding

The DC supply ground may be shorted to the RF ground of the SMA connector.

4. Experimental Environments on Site

The following equipment will be prepared by the SYDC committee for the evaluation at the competition:

(a) A vector network analyzer

(b) Power supply for collector, base bias, and ground through respective female banana plugs

The attendee must complete the measurement within the specified time limit.